## IN THE CLAIMS

Please amend the claims as follows:

In the following claims, claims 1, 4, 8, 10, 11, 12, 13 and 16 are amended for clarity and not for reasons of patentability. Claims 19 and 21 are amended simply to replace the claim dependency with the full text of claims 16 and 18 and claim 16 respectively and not for reasons of patentability.

1. (Currently Amended) A parallel counter comprising:

~~a plurality of~~ at least five inputs for receiving a binary number as a plurality of binary inputs;

~~a plurality of~~ at least three outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating ~~each of the plurality of~~ at least three of the binary outputs as ~~a~~ elementary OR or EXOR symmetric ~~function~~ functions of the binary inputs, wherein the elementary OR symmetric function comprises the result of OR logic combining binary inputs to generate a binary output which is high if and only if m >1 or AND logic combining sets of binary inputs and OR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and the elementary EXOR symmetric function comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or AND logic combining sets of one or more binary inputs and EXOR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) A parallel counter according to ~~claim 3~~ claim 1 wherein said logic circuit is arranged to at least one of: generate the first and least significant bit of the binary output by EXOR logic combining the binary inputs; and generate the $(i+1)^{th}$ binary output by ~~logically~~ AND logic combining $2^i$ of the binary inputs in each set and EXOR logic combining the result of the AND logic combinations ~~for the generation of the $i^{th}$ binary output~~, where i is an integer from 1 to N-1, N is the number of binary outputs and i represents the significance of [each] a binary output, each set being unique and the sets covering all possible combinations of binary inputs.

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Currently Amended) A parallel counter according to ~~claim 7~~ claim1 wherein said logic circuit is arranged to logically AND $2^{N-1}$ of the binary inputs in each set ~~for~~ in the generation of the $N^{th}$ binary output as the elementary OR symmetric function of the binary inputs, where N is the number of binary outputs and the $N^{th}$ binary output is the most significant, each set being unique and the sets covering all possible combinations of binary inputs.

9. (Canceled)

10. (Currently Amended) A parallel counter according to claim 1 wherein said logic circuit is arranged to generate a first binary output ~~as a~~ as an elementary EXOR symmetric function of the binary inputs ~~using exclusive-OR logic for combining a plurality of sets of one or more binary inputs~~, and to generate an $N^{th}$ binary output ~~as a~~ as an elementary OR symmetric function of the binary inputs ~~using OR logic for combining a plurality of sets of one or more binary inputs~~.

11. (Currently Amended) A parallel counter according to claim 1 wherein said logic circuit is arranged to generate two possible binary outputs for a binary output less significant than the $N^{th}$ binary output, as elementary OR symmetric functions of the binary inputs ~~using OR logic for combining a plurality of sets of one or more binary inputs~~, where N is the number of binary outputs, the sets used for each possible binary output being of two different sizes which are a function of the binary output being generated; and said logic circuit including selector logic to select one of the possible binary outputs based on a more significant binary output value.

12. (Currently Amended) A parallel counter according to claim 11 wherein said logic circuit is arranged to generate the two possible binary outputs for the $(N-1)^{th}$ binary output less significant than the $N^{th}$ binary output, as elementary OR symmetric functions of the binary inputs ~~using OR logic for combining a plurality of sets of one or more binary inputs~~, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and $2^{N-2}$ respectively and said selector logic being arranged to select one of the possible binary outputs based on the $N^{th}$ binary output value.

13. (Currently Amended) A parallel counter according to claim 1 wherein said logic circuit includes a plurality of subcircuit logic modules each generating intermediate binary outputs ~~as a~~ as an elementary OR or EXOR symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

14. (Canceled)

15. (Canceled)

16. (Currently Amended) A logic circuit for multiplying two N bit binary numbers, the logic circuit comprising:

array generation logic for performing a first stage of logical combining by performing the logical AND operation between each bit in one binary number and each bit in the other binary number to generate an array of logical AND combinations comprising an array of binary values, and for performing a second stage of logical combining by ~~further~~ logically combining ~~values~~

AND combinations to ~~generate the~~ generate an array in which the maximal depth of the array is below N bits;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers.

17. (Canceled)

18. (Canceled)

19. (Currently Amended) A logic circuit ~~according to claim 18 wherein said generation logic is arranged to combine the combinations~~ for multiplying two N bit binary numbers, the logic circuit comprising:

array generation logic arranged to logically AND combine each bit $A_i$ of a first binary number with each bit $B_j$ of a second binary number to generate an array comprising a sequence of binary numbers represented by said logical AND combinations, $A_i$ AND $B_j$ , and to carry out further logical combinations by logically combining the combinations $A_1$ AND $B_{N-1}$ and $A_0$ AND $B_{N-2}$ , $A_1$ AND $B_{N-2}$ and $A_0$ AND $B_{N-1}$ using exclusive OR logic to replace $A_1$ AND $B_{N-2}$ combination ~~these combinations~~, and to combine $A_1$ AND $B_{N-1}$ and $A_0$ AND $B_{N-2}$ to replace the $A_1$ AND $B_{N-1}$ combination to generate an array in which the maximal depth of the array is below N bits, where N is the number of bits in the binary numbers and i and j are integers from 1 to N;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers.

20. (Original) A logic circuit according to claim 16 wherein said array reduction logic includes at least one of: at least one full adder, at least one half adder, and at least one parallel counter.

21. (Currently Amended) A logic circuit ~~according to claim 20~~ for multiplying two N bit binary numbers, the logic circuit comprising:

array generation logic for performing a first stage of logical combining by performing the logical AND operation between each bit in one binary number and each bit in the other binary number to generate an array of logical AND combinations comprising an array of binary values, and for performing a second stage of logical combining by logically combining AND combinations to generate an array in which the maximal depth of the array is below N bits;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter according to [any one of] claim[s] 1, 4, 8, 10, 11, 12, or 13 ~~to 15~~.